



## ***AMS: Chip design for automotive applications and layout guidelines for ESD/LU robustness***

### ***Abstract:***

This presentation will start with a brief overview of AMS company in general, concerning the supported market segments and applications, and the design center in Pavia in particular. The seminar will be organized in two parts: the first part will be focused on automotive electronics, the segment of interest developed in Pavia. Starting from the definition of main general requirements for automotive device, general guidelines and required analyses will be derived, which need to be taken into account during the development of a typical automotive project.

The second part will be focused on a general presentation of a proposed layout strategy to follow to achieve good ESD/LU robustness: a layout work flow and some tips will be presented to reduce the risk of incurring into ESD/LU problems in the final device.

In the end there will be some time for Q&A on each of the two parts of the seminar.

### ***Speakers:***

**Marco Cerchi** graduated in Electronic Engineering from University of Pavia. From 2000 to 2001 he was Analog Designer at ST-Microelectronics, developing high-frequency sigma-delta D/A converters and PLLs. In 2001 he joined MIKRON-Italy working on IC design for battery charge solutions and sensor interface ASICs (smoke detectors, touch-screens, bar-code readers). In 2004 he moved to AUSTRIAMICROSYSTEMS Italy (AMS Italy since 2012), as Analog Designer, developing SL LDOs,  $\mu$ Processor supervisors and Hall effect magnetic position sensors. Since 2016 he is Engineering Manager in AMS Italy, Pavia

**Simone Verri** received the Diploma Degree in Electronic Engineering from University of Pavia. From 1998 to 2000 he was Layout Engineer at ST-Microelectronics, developing ICs in BCD3, BCD5 and HF5CMOS for Industrial & Power Supply applications. In 2000 he joined MIKRON Italy working on ASIC design in XC06, CX08, CX08H (XFAB) and 0.5um 2P3M polycide 5V/3.3V (TSMC) technologies. From 2005 he is Senior Layout Engineer at AUSTRIAMICROSYSTEMS Italy (AMS Italy since 2012) developing SL LDOs,  $\mu$ Processor supervisors and DCDC converters, automotive ASICs in C35, H35 and H18 processes

**The seminar will be Dec. 13, from 4:00 to 6:00 PM, in the Seminar Room Floor D.**

