



Analog Mixed-Signal IP Challenges in “Big Digital” SoCs

September 22nd, h 11.00, Magenta Seminar Room (D Floor)

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Abstract: The presentation will highlight some of the challenges associated with designing and integrating essential analog blocks (bias references, sensors, frequency synthesizers) into very large SoCs on the latest FinFET nodes. Issues such as stringent layout rules, process effects, efficient technology porting, routing challenges and the importance of yield will all be addressed.

Speakers: Stefano Facchin, Przemyslaw Mrosczczyk (Qualcomm, Cork Design Centre)