UNIVERSITÀ DI PAVIA
Department of Electrical, Computer and Biomedical Engineering
PHD SCHOOL IN MICROELECTRONICS

IEEE SOLID-STATE CIRCUITS SOCIETY
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Italian Chapter

On-Chip Self-Interference Mitigation for Integrated Systems

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Abstract: *Several efforts of the last decade have demonstrated the ability of a radio transceiver to simultaneously transmit and receive using the same frequency band – this is commonly referred to as in-band full duplex communication. Numerous performance challenges are presented to the analog, mixed-signal and digital IC designers when attempting to realize an integrated full duplex radio. Specifically, the strong transmitter self-interference will degrade the RX SNDR which is impacted by a number of performance issues including receiver linearity and noise figure degradation, reciprocal mixing, demand for high cancellation bandwidth and depth, in addition to algorithms to adapt and optimize suppression circuits in real-time. Although the last few years research on circuits and systems which enable full duplex radio communication have been widely published, the topic of self-interference cancellation is by no means limited to wireless communication systems. In fact, many other commercial and biomedical applications benefit from the ability to suppress transmitted/emitted signals in a system that is attempting simultaneously receive another signal. Examples include neural interfaces, radar, wireline communication and medical imaging. This presentation will begin by exploring the similarity and differences between the problem of self-interference/signal cancellation in very diverse applications from the perspective of noise, linearity, cancellation bandwidth, convergence of adaptation algorithms and suppression depth. Then two examples of integrated self-interference cancellation will be presented for neural interfaces and wireless communication which represent the state-of-the-art with respect to linearity, noise and the ability to adapt cancellation filters on chip in real-time.*

Speaker: Chris Rudell, Associate Professor, University of Washington

Jacques "Chris"tophe Rudell received degrees in electrical engineering from the University of Michigan (BS), and UC Berkeley (MS, PhD). After finish his PhD, he worked for several years as an RF IC designer at Berkana Wireless (now Qualcomm), and Intel Corporation. In January 2009, he joined the faculty at the University of Washington, Seattle, where he is now an Associate Professor of Electrical and Computer Engineering. He is also a member of the Center for Neural Technology (CNT) and serves as the co-director of the Center for Design of Analog-Digital Integrated Circuits (CDADIC).

While a PhD student at UC Berkeley, Dr. Rudell received the Demetri Angelakos Memorial Achievement Award, a citation given to one student per year by the EECS department. He has twice been co-recipient of the best paper awards at the IEEE International Solid-State Circuits Conference, the first of which was the 1998 Jack Kilby Award, followed by the 2001 Lewis Winner Award. He received the 2008 ISSCC best evening session award, and best student paper awards at the 2011 and 2015 RFIC Symposium. Chris is the recipient of the National Science Foundation (NSF) CAREER Award. Dr. Rudell served on the ISSCC technical program committee (2003-2010), and on the *IEEE Radio Frequency Integrated Circuits* (RFIC) Symposium steering committee (2002-2013), where he was the 2013 General Chair. He was an Associate Editor for the *IEEE Journal of Solid-State Circuits* (2009-2015). At present, he serves on the technical program committees of the *IEEE European Solid-State Circuits Conference* (ESSCirC) and the *IEEE Custom Integrated Circuits Conference* (CICC).