University of Pavia

Ph.D. School in Electronics, Computer Science and Electrical Engineering
Ph.D. School in Microelectronics

Total Ionizing Dose Degradation Mechanisms in Nanometer-scale Microelectronic Technologies

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Abstract: This talk presents the total ionizing dose (TID) degradation mechanisms in several modern nanometer-scale technology nodes, ranging from 150 nm, 65 nm and 28 nm Si MOSFET, to 16 nm InGaAs FinFET. The analysis of the TID mechanisms is focused on the evaluation of measurable effects affecting the electrical response of the devices and on the identification of the microscopical nature of the radiation-induced defects. Various transistors, based on MOSFET and FinFET structures of different manufacturers, were tested under ionizing radiation at several temperatures, bias configurations, annealing conditions, and transistor sizes. Technologies dedicated to high energy physics experiments were tested at ultra-high doses, never explored thus far. Different techniques, as DC static characterization, charge pumping and low frequency noise measurements, as well as Technology Computer-Aided Design simulations, were used to identify location, density and energy levels of the radiation-induced defects. All results confirm the high TID tolerance of the thin gate oxide of nanoscaled technologies, due to the reduced charge trapping in the gate dielectric. On the other hand, the aggressive downsizing of devices has led to new TID-induced effects related to other thick oxides and modern production processes, e.g., shallow trench insulations oxides, spacer dielectrics, and halo implantations.

Organizer

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The seminar will take place in English
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