Introduction to DSP based Serial Links

Abstract. We introduce the design challenge of implementing a Serializer/Deserialized (SerDes) system capable of sustaining a bitrate >50 Gb/s and 100Gb/s. The switch from an NRZ to a PAM-4 modulation scheme, with the increased equalization power required on the receive side, encourages the adoption of DSP based solutions to implement current and next generations long reach SerDes. There are two big challenges to be coped with, power consumption due to digital domain signal processing, and the complexity of designing the Analog Front End capable of converting A/D and D/A at the required sampling frequency. A holistic approach implying the codesign of the AFE and DSP, including an embedded software component as firmware, has been taken to provide a very efficient and powerful implementation in 7nm. The second part of the talk gives some details of the architecture and performance as presented at this year's ISSCC, showing how both power consumption and channel length are widely improved over previous works. Paper title is: "A sub-250mW 1.25-to-56Gb/s continuous range PAM-4 42.5dB IL ADC/DAC-based transceiver in 7nm FinFET"

About eSilicon. eSilicon provides complex FinFET ASICs, market-specific IP platforms and advanced 2.5D packaging solutions. Our ASIC-proven, differentiating IP includes highly configurable 7nm 56G/112G SerDes plus networking-optimized 16/14/7nm FinFET IP platforms featuring HBM2 PHY, TCAM, specialized memory compilers and I/O libraries.

Speakers

Matteo Pisati received the M.Sc. and the Ph.D. degrees in electrical engineering from the University of Pavia, Italy, in 2001 and 2005, respectively. During his Ph.D., he worked on CMOS analog circuits for Clock and Data Recovery applications. From 2005 to 2012 he was with ST-Microelectronics, working as analog designer in the High Speed Serial Interface group. From 2012 to 2017 he worked for Marvell Semiconductor as project leader of the DSP-based PAM4 SerDes project. He is now Senior Manager at eSilicon, where he is leading the development of the 56Gb/s Serdes project.

Fernando De Bernardinis received the Laurea degree in electrical engineering from the University of Pisa, Scuola S. Anna, Italy, in 1996, a Ph.D in Electrical Engineering from the same University in 2000 and M.S. and Ph.D. degrees from the University of California, Berkeley, in 2001 and 2005, respectively. He was Assistant Professor in the Department of Information Engineering at the University of Pisa until he joined Marvell Italy in 2006 and eSilicon in 2017. His research interests include digitally assisted analog design, mixed signal system level design, architecture design and DSP algorithm optimization. Since 2012, he has been leading the architecture and algorithm design of DSP based serial links, developing 56 Gb/s and 112Gb/s generations at eSilicon.

The seminar will be Monday, April 15th 2019, from 4 to 6 PM, Seminar Room floor D