A 64Gb/s Low-Power Transceiver for Short- Reach PAM-4 Electrical Links in 28nm FDSOI CMOS

Abstract:A PAM-4 transceiver operating up to 64Gb/s in 28nm CMOS FDSOI for short-reach electrical links is presented. Receiver equalization relies on a flexible CTLE, providing a very accurate channel inversion through a transfer function that can be optimally adapted at low, mid and high frequency independently. The CTLE meets the performance requirements of CEI-56G-VSR without requiring DFE implementation. As result, timing constraints for comparators in data and edge sampling paths may be relaxed by using track-and-hold stages, saving power consumption. At the maximum speed, the receiver draws 180mA from 1V supply, corresponding to 2.8mW/Gb/s only. The transmitter embeds a flexible FFE which can be reconfigured to comply with legacy standards. A comparison between current- and voltage-mode TX drivers is proposed, proving through experiments that the latter yields larger PAM-4 eye openings thanks to the intrinsically higher speed. The full transceiver (TX, RX and clock generation) operates from 16Gb/s to 64Gb/s in PAM-4, 8Gb/s to 32Gb/s in NRZ, and supports 2x and 4x oversampling to reduce data rate down to 2Gb/s. A TX-to-RX link at 64Gb/s, across a 16.8dB-loss channel, reaches 10-12 minimum BER and 0.19UI horizontal eye opening at BER=10-6, with 5.02mW/Gb/s power dissipation.

Speakers:

E. Depaoli was born in Pavia, Italy, in 1980. He received the Laurea degree in electronics engineering from the University of Pavia, Italy, in 2004. His Laurea thesis focused on the study of a RF Front-End for Multistandard Simultaneous or Alternative Receiver Based on LNA with Positive Feedback. In 2004-2005 he was involved in the FIRB project in the design of a multistandard receiver for WLAN. In december 2005 he joined STMicroelectronics in Pavia in "Studio di Microelettronica" as analog design engineer in the New IP & Design Support Group. He is currently the analog project leader of the High Speed interface design team. His current research interests inlude the development of IPs for high-speed serial links.

G. Albasini was born in Voghera, Italy, in 1974. He received the Laurea degree in electronics engineering from the University of Pavia, Pavia, Italy, in 1999, and the Executive MBA degree from Stogea, Bologna, Italy, in 2004. In 2000, he joined STMicroelectronics, Pavia, where he was involved in RF analog design for radio communications. In 2002, he joined IMEC, Leuven, Belgium, where he was involved in system analysis for WLAN. Since 2007, he has been a Design Manager within STMicroelectronics, leading many innovative projects, in the field of millimeter-wave, UWB, probe storage, and HDD, and achieving many silicon successes. In the last years his research interests have included high-speed serial interfaces, particularly for BaseT Ethernet and SerDes applications.

The seminar will be **May 6th** 2019, from **4 to 6 PM** in the **Magenta Seminar Room, Floor D** of the Department of Electrical, Computer and Biomedical Engineering.