University of Pavia
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SEMINAR

"On-chip active delay lines with widely tunable delays"

Prof. Nagendra Krishnapura
Indian Institute of Technology Madras
Chennai, India

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Abstract: *An all-pass filter architecture that can be generalized to high orders, and can be realized using active circuits is proposed. Using this, a compact true-time-delay element with a widely tunable delay and a large delay- bandwidth product is demonstrated. This is useful for beamforming and equalization in the lower GHz range where the use of LC or transmission line based solutions to realize large delays is infeasible. Coarse tuning of delay is realized by changing the filter's order while keeping the bandwidth constant and fine tuning is implemented by changing the filter's bandwidth utilizing the delay-bandwidth trade-off. A test chip fabricated in 130nm CMOS process demonstrates a delay tuning range of 0.25 to 1.7ns over a bandwidth of 2GHz, while maintaining a magnitude deviation of +/-0.7 dB. The filter has a worst case noise figure of 23dB, and -40dB IM3 distortion for 37 mV ppd inputs. The chip dissipates 112 to 364 mW of power between its minimum and maximum delay settings. Computed radiation pattern with four antennas spaced λ(fmax)/2 apart shows +/-90 degree beam steering off broadside. The filter's delay-bandwidth product of 3.4, which, combined with a small active area of 0.6mm^2, corresponds to a substantial improvement over the state-of-the-art of on-chip active delay lines.*

Bio: Nagendra Krishnapura received the B.Tech. degree from IIT Madras, India, and the Ph.D. degree from Columbia University, New York City, NY, USA.
During his Ph.D. he worked under the guidance of Prof. Yannis Tsividis in the area of nonlinear analog signal processing for low power integrated circuits.
He was an Analog Design Engineer at CeLight Inc., Multilink, and Vitesse semiconductor.
He has taught analog circuit design courses at Columbia University as an Adjunct Faculty.
He is currently an Associate Professor with IIT Madras. His research interests are analog and RF circuit design and analog signal processing.

Organizers

Prof. Danilo Manstretta

Ph.D. Coordinator

Prof. Guido Torelli

Seminar in English

For more information: danilo.manstretta@unipv.it