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Dissecting Design Choices for Power Efficient Continuous-time Delta Sigma Analog-to-Digital Converters

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Abstract - *Continuous-time Delta-Sigma Modulators (CTDSMs) are a compelling choice for the design of high resolution analog-to-digital converters. Many delta-sigma architectures have been published (and continue to be invented). This leaves the designer with a bewildering array of choices, many of which seem to pull in opposite directions. Further, it is often difficult to make a clear comparison of various architectures, as they have been designed for dissimilar specifications, by different design groups, and in different technology nodes. This talk examines various alternatives for the design of power efficient single-loop continuous-time delta sigma converters.*

Bio - Shanthi Pavan received the doctoral degree from Columbia University, New York City, in 1999. He is currently a Professor of Electrical Engineering. He is the author of *Understanding Delta-Sigma Data Converters* (Second Edition), with Richard Schreier and Gabor Temes. His research interests are in the areas of high speed analog circuit design and signal processing.

He is a recipient of many awards, including the IEEE Circuits and Systems Society Darlington Best Paper Award (2009) and the Shanti Swarup Bhatnagar Award (2012). He has served as an Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS: REGULAR PAPERS. He has been on the Technical Program Committee at the International Solid-State Circuits Conference, and a Distinguished Lecturer of the Solid-State Circuits Society. He is a distinguished lecturer of the IEEE Circuits and Systems Society, and an IEEE Fellow.

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