University of Pavia
Ph.D. School of Microelectronics

SEMINAR
"Xilinx FPGA in High Speed Serial Links"

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Abstract: *The proliferation of modern-day mobile communication devices has created an explosion in bandwidth requirements for the communication infrastructure. Supporting this infrastructure requires an ability to process large volumes of data as well as transport the data between devices. FPGAs (Field Programmable Gate Array) have evolved significantly from their initial conception as programmable logic device to support the modern-day communication requirements. The evolution has been possible as a result of process technology scaling and significant new functionality that has been added to FPGAs. The architecture of FPGA supports a huge degree of parallelism and, with the ability to be rapidly reprogrammed, they are well suited to supporting different application requirements. FPGAs provide a very efficient means of processing large amounts of data. It is vital that the data pipe to and from the FPGA has sufficient capacity to take advantage of the processing power. A significant hurdle in communication links is the frequency-dependent loss of the communication channel, which leads to higher loss at higher data rates. In order to support the required data throughput of modern communication systems without increasing channel cost significantly, there has been significant development in SerDes technology. SerDes uses a number of techniques to transmit and receive serial data reliably. This solution is more cost effective than improving the channel loss or increasing the number of channels in parallel. Xilinx designs and deploys SerDes in their FPGAs, to make them more suitable in applications requiring high speed serial links.*

Bio: Frantz Stephane Ngankem received the bachelor's degree of electronic and telecommunication engineering from the University of Pavia in 2013 and the master's degree of electronic engineering (with focus on microelectronics) from the same university in 2015. As part of his master's degree, he was an intern as an Analogue Mixed Signal Design Engineer for battery management systems in Freescale Semiconductor of Toulouse in France (now NXP).
In 2016, he joined Xilinx, Ireland, Cork, as an Analogue Design Engineer with the SerDes technology group, where he has been involved in the design of circuits for high-speed serial links.
He is interested in the areas of high-speed circuit design, DACs, ADCs and PLLs.

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