eSilicon meets Pavia University @ Industrial Topics Seminars

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4-6 PM, SEMINAR ROOM FLOOR D

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Abstract

In the first part of this presentation we'll introduce eSilicon corporation, what we do in eSilicon and how we do it as a global enterprise.

We will than focus on eSilicon Pavia site core expertise, the design of High Speed SerDes.

We will get a glimpse on how we are organized in Pavia, how much we want to grow and what professionals skills we are looking for.

In the second part of the presentation will focus on two design examples to show what it takes, from a very technical perspective, to develop state of the art products.

Technical experts of eSilicon Pavia will talk about a very efficient High Speed ADC that enable efficient large bandwidth data processing and on our 56GSps PAM4 SerDes prototype.

Presenter's Profile

Giovanni Cesura received the M.Sc. and the Ph.D. degrees in electrical engineering from University of Pavia Italy , in 1989 and 1993 respectively. From 1993 to 1997 he was with Max Plank Institute in Munich to develop detectors and read-out electronics for LHC accelerator at CERN. In 1997 he joined STMicroelectronics were he worked on the design of Audio Delta-Sigma ADC, in 2000 he was the co-director of the Studio di Microelettronica were he was in charge for the development of high speed ADCs and DACs for wired and wireless communication. In 2005 he joined Marvell Italy as director of Analog IP development. Since 2017 he is with eSilicon leading the Analog Design and Custom Layout team of the SerDes development group in Pavia.

Nicola Ghittori received the M.Sc. and the Ph.D. degrees in electrical engineering from the University of Pavia, Italy, in 2002 and 2006, respectively. During his Ph.D., he worked on CMOS analog circuits for wireless transceivers and analysis of package and substrate crosstalk in mixed-signal integrated circuits. He is currently with eSilicon Italy, as an Analog IC Design Engineer. His main interests are in high-speed and high-performance analog/mixed-signal circuit design.

Claudio Nani was born in Brescia, Italy, in 1983. He received his M.sc. in electrical engineering from University of Pisa and Scuola Superiore Sant'Anna in 2007 and 2008 respectively. From 2007 to 2010, he was with the Mixed Signal Circuits and Systems group of NXP Semiconductors Research, Eindhoven (The Netherlands) where he worked on high-speed ADC for cable tuners applications. From 2010 to 2017 he was with Marvell, Pavia (Italy) where he was involved in the design of high performance data converters for telecommunications systems. In 2017 he joined eSilicon, Pavia (Italy) working on high speed ADC and analog front end for wireline interfaces. His current research interests include high-speed power-efficient ADCs, data converter digital calibration systems and high performance wireline interfaces.

Technical Talks

A 0.076mm2 12b 26.5mW 600MS/s 4-way Interleaved Sub-ranging SAR-$\Delta\Sigma$ ADC with on-chip buffer in 28nm CMOS

Abstract

A 0.076mm^2 12b 28nm 600MS/s 4 way time interleaved ADC with on chip buffer is presented. The usage of a sub-ranging architecture consisting of a coarse SAR ADC followed by an incremental DS fine converter enables significant power reduction compared to conventional SAR. The ADC area has been optimized by adopting a segmented Charge-Sharing Charge-Redistribution DAC. The ADC and buffer prototype achieves an SNDR of 60.7dB and 58dB at low and high frequency respectively while consuming only 26mW.

High Speed Serial communication. The main challenges of a 56Gb/s PAM4 ADC based Networking SerDes

Abstract

In this talk we will first present the key concepts of high speed serial communications and introduce the basic transceivers block diagrams with specific focus on ADC based receivers architectures. We will dive into the details of the main challenges involved in the design of high speed ADCs used in these application and review the different ADC architectures options. Afterward the architecture and key performance of a 28nm 56Gb/s PAM4 ADC based Serdes employing a 8b 28GS/s 48-way Time Interleaved SAR ADC will be presented.


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